CLAIMS

What is claimed is:

1. A register file comprising:

   a dynamic local bit trace;

   a plurality of data cells coupled to the dynamic local bit trace; and

   a device coupled to the dynamic local bit trace to facilitate precharging the dynamic local bit trace to a precharge value and to intelligently hold the precharged value on the dynamic local bit trace during evaluation of the dynamic local bit trace.

2. The register file of claim 1 wherein intelligently holding the precharged value on the dynamic local bit trace comprises selectively coupling and decoupling a driving signal trace from the dynamic local bit trace.

3. The register file of claim 2 wherein selectively coupling and decoupling comprises coupling and decoupling the driving signal trace from the dynamic local bit trace based on address information associated with the plurality of data cells.

4. The register file of claim 2 wherein the driving signal trace is coupled to a power supply.

5. The register file of claim 1 wherein the device comprises a PMOS transistor.

6. The register file of claim 5 wherein a drain of the PMOS transistor is coupled to a driving signal trace and a source of the PMOS transistor is coupled to the dynamic local bit trace.

7. The register file of claim 1 wherein the device comprises an NMOS transistor.

8. The register file of claim 1 further comprising device control logic coupled to the device.

9. The register file of claim 8 further comprising:

a clock signal trace coupled to the device control logic; and

a select signal trace coupled to the device control logic.

10. The register file of claim 9 further comprising decode logic coupled to the select signal trace to provide an indication of an access to one of the plurality of data cells.

11. The register file of claim 10 further comprising a plurality of address signal traces coupled to the decode logic, wherein the provision of an indication of an access is based at least in part a subset of the plurality of address signal traces.

12. The register file of claim 11 wherein said subset of the plurality of address signal traces includes one or more most significant bits of the address signal traces.

13. The register file of claim 1 further comprising a domino keeper coupled to the dynamic local bit line.

14. A register file comprising:

a dynamic local bit trace;

a plurality of data cells coupled to the dynamic local bit trace; and

a device coupled to the dynamic local bit trace to facilitate precharging the dynamic local bit trace to a precharge value and to selectively couple and decouple a driving signal trace from the dynamic local bit trace to hold the precharged value on the dynamic local bit trace during evaluation of the dynamic local bit trace.

15. The register file of claim 14 wherein selectively coupling and decoupling comprises coupling and decoupling the driving signal trace from the dynamic local bit trace based on address information associated with the plurality of data cells.

16. The register file of claim 15 further comprising a domino keeper coupled to the dynamic local bit line.

17. A register file comprising:

a dynamic local bit trace;

a precharge device coupled to the dynamic local bit trace;

a plurality of data cells coupled to the dynamic local bit trace; and

a device coupled to the dynamic local bit trace to intelligently hold a precharged value on the dynamic local bit trace.

18. The register file of claim 14 further comprising decode logic coupled to the device to provide an indication to the device of an access to one of the plurality of data cells.

19. The register file of claim 18 further comprising a plurality of address signal traces coupled to the decode logic, wherein the provision of an indication is based at least in part a subset of the plurality of address signal traces.

20. A register file comprising:

a first and a second dynamic local bit trace;

a first and a second plurality of data cells correspondingly coupled to the first and the second dynamic local bit traces;

a first and a second device correspondingly coupled to the first and the second dynamic local bit traces to facilitate precharging the first and the second dynamic local bit traces to a precharge value and to

intelligently hold the precharged value on the first and the second dynamic local bit traces during evaluation of the first and the second dynamic local bit traces; and

global multiplexing logic coupled to the first and the second dynamic local bit traces to facilitate provision of a data value corresponding to an accessed data cell on an output signal trace.

21. The register file of claim 20 wherein intelligently holding the precharged value on the first and the second dynamic local bit traces comprises selectively coupling and decoupling a driving signal trace from the first and the second dynamic local bit traces.

22. The register file of claim 20 further comprising a first and a second device control logic correspondingly coupled to the first and the second device.

23. The register file of claim 22 further comprising:

a first and a second clock signal trace correspondingly coupled to the first and the second device control logic; and

a first and a select signal trace correspondingly coupled to the first and the second device control logic.

24. The register file of claim 23 wherein the first and the second clock traces comprise a single clock trace.

25. The register file of claim 23 further comprising decode logic coupled to the first and the second select signal trace to provide an indication of an access to one data cell of the first and the second plurality of data cells.

26. The register file of claim 25 further comprising a plurality of address signal traces coupled to the decode logic, wherein the provision of an indication of an access is based at least in part a subset of the plurality of address signal traces.

27. The register file of claim 20 wherein at least one of the first and the second device comprises a PMOS transistor and wherein a drain of the PMOS transistor is coupled to a driving signal trace and a source of the PMOS transistor is coupled to the respective dynamic local bit trace.

28. A system comprising:

a processor including;

a register file comprising:

a first and a second dynamic local bit trace;

a first and a second plurality of data cells correspondingly coupled to the first and the second dynamic local bit traces;

a first and a second device correspondingly coupled to the first and the second dynamic local bit traces to facilitate precharging the first

and the second dynamic local bit traces to a precharge value and to intelligently hold the precharged value on the first and the second dynamic local bit traces during evaluation of the first and the second dynamic local bit traces; and

global multiplexing logic coupled to the first and the second dynamic local bit traces to facilitate provision of a data value corresponding to an accessed data cell on an output signal trace;

a memory configured to store data; and

a bus coupled to the processor and memory to facilitate data exchange between the processor and memory.

29. The system of claim 28 wherein intelligently holding the precharged value on the first and the second dynamic local bit traces comprises selectively coupling and decoupling a driving signal trace from the first and the second dynamic local bit traces.

30. The system of claim 28 wherein the register file further comprises a first and a second device control logic correspondingly coupled to the first and the second device.

31. The system of claim 30 wherein the register file further comprises:

a first and a second clock signal trace correspondingly coupled to the first and the second device control logic; and

a first and a select signal trace correspondingly coupled to the first and the second device control logic.

32. The system of claim 31 wherein the first and the second clock traces comprise a single clock trace.

33. The system of claim 31 wherein the register file further comprises decode logic coupled to the first and the second select signal trace to provide an indication of an access to one data cell of the first and the second plurality of data cells.

34. The system of claim 33 wherein the register file further comprises a plurality of address signal traces coupled to the decode logic, wherein the provision of an indication of an access is based at least in part a subset of the plurality of address signal traces.